Study of the Interconnect Failure Mechanism and Micro-effort for ULSI

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Abstract: Interconnect reliability has been regarded as a discipline that must be seriously taken into account from the early design phase of ultra large scale integration (ULSI). A synthetic review of valuable solutions to improve interconnect reliability is proposed in this paper. At first, a comprehensive review of the interconnect failure mechanisms and micro-efforts are carried out. Four types of interconnect failure mechanisms including EM, SM, TM and TDDB are illustrated in detail. Depending on their different effects for failure, the interconnect micro-effects are classified into the positive effects including the short-length effect, self-healing effect, reservoir effect and the negative effects which involves the skin effect, joule heating, current crowding , bandwidth, coupled noise, parasitic, RC delay, crosstalk and power dissipation and so on. Secondly, a novel qualitative evaluation method based on the radar chart has been presented, which visually shows the contrast of the key performance related to the interconnect failures. These present results might provide some valuable guidance for the study of IC interconnect reliability.

Key words: Ultra large scale integration (ULSI), electromigration, interconnect reliability, RC delay, failure mechanisms, micro-effects.

1. Introduction

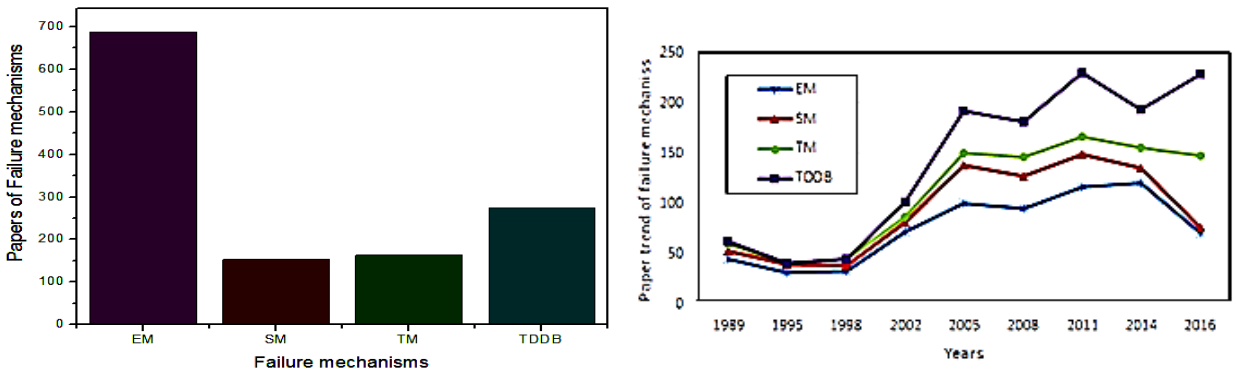
Wireless communications has revolutionized the whole society, from satellite transmission, radio and television broadcasting to the ubiquitous mobile telephone. Meanwhile, the microelectronics industry continues to push for higher performance and downscaling of device dimensions, leading to an increase in current density for metallic interconnects. All these revolutions need plenty of ultra large scale integration which are a set of circuits on one small chip of semiconductor material. Modern ICs can be made by incorporating up to several billions transistors and the components in a relative small area. With the advent of 4G era, the frequency and current density of IC increase dramatically. Hence, integrated circuits (ICs) reliability is increasingly important as our reliance on electronic products has increased tremendously today in our daily lives. Furthermore, all the transistors and components have to be electrically interconnected to provide the proper functionality in ULSI. Interconnect reliability has attached increasing importance, especially when the line width becomes narrower that renders high current density as shown by Srinivasan [1]. Meanwhile, interconnect reliability has become crucial and affected the performance, power consumption and reliability of the whole circuit as the IC undergoes continued downscaling according to the Moore's law [2]. Some new problems such as the increase of interconnect parasitic,

crosstalk and noise cannot be neglected and become the new challenges for interconnect reliability [3].

In this case, the main interconnect failure mechanisms and micro-effects are summarized here, which are closely related to some factors such as current density, temperature, width and so on. In order to evaluate the interconnect reliability, how to measure the impacts of failure mechanisms, micro-effects and the related factors on interconnect reliability should be considered. Furthermore, a novel qualitative evaluation method has been presented, which show their influences on interconnect reliability visually. This paper is arranged as following, the failure mechanisms and micro-effects have been summarized in Section II. A novel method to evaluate the interconnect reliability is presented in Section III. Finally, the conclusion is given in the Section IV.

2. Interconnect Failure Mechanisms and Micro-effects

With the advent of nanometer era, it needs large quantity of complex interconnects to connect highly integrated chip with the other electronic components. In view of the above-mentioned, interconnect reliability must be addressed. In order to analysis the interconnect reliability, it is extremely necessary to find out the reasons and influence factors for the IC interconnect failure. In this part, the failure mechanisms and micro-effects of interconnect are analyzed. One of the goals is to identify the failure mechanisms and their impacts on the interconnect properties.



(a) The number of papers for failure mechanisms (b) The paper distribution of failure mechanisms

Fig. 1. The statistic for interconnect failure mechanisms.

2.1. Interconnect Failure Mechanisms

With the increase of failure rate, to identify the failure mechanism is the key to ensure reliability. There are mainly four types of interconnect failure mechanisms [4] including EM, SM, TM and TDDB. The paper statistic is investigated in Fig. 1(a) and (b), which indicates that EM is the most significant threat for interconnect reliability in the high performance IC.

2.1.1. EM failure

With the continuous improvement of integration level, the feature size is scaling constantly, but the current density has not scaled proportionally. The high current density makes the interconnect line susceptible to EM. When the film is stressed with high current density (>105A/cm2), the remarkable mass transport leads to accumulation of vacancies or atoms and creates voids or hillocks in interconnect [5]. The void formation in interconnect would cause the open circuit and even catastrophic disconnections [6]. The hillocks would result in shorts between wires. EM failure behaves as resistance increase, void throughout to form open circuit and atomic pile up to form the hill or whisker [7]. The short circuit between layers occurs and penetrates the passivation layer forming the corrosion source with the growth up of hill or whisker [8].

EM is a complex multi-physics problem including electrical, thermal and mechanical. Since EM failure had been found in the 60's, research on EM has progressed significantly and the physics theory was well established. The first report on EM was presented by Fiks in 1959 [9]. Then, Huntington and his coworkers contributed to EM failure and proposed that electron wind force was taken as the only driving force for EM mass transport [10]. The reduction in line width and the increase of temperature gradient which is caused by the changes of temperature and mechanical stress gradient are the major reasons for EM [11]. Tan investigated the influence of temperature and stress gradient for the Cu narrow interconnect [12]. Then Arzt and Kraft studied the effect of surface tension gradient in EM. Later, Dalleau combined these driving forces to analysis EM in Al considering voids dynamic growth [13]. The work by Li showed that current density was no longer the sole driving force for EM when the line width became less than 0.20μm.

EM failure is generally described by the famous Black equation which is used to determine the maximum current density flowing in a wire safely. In 1969, Black proposed the classic EM failure time formula, it can be written as equation (1) [14], where A is a constant based on interconnect geometry and material, j is the current density, Q is the activation energy (0.5eV for Cu and Al alloys), K_B is the Boltzmann constant and T is the temperature.

$$MTF = Aj^{-2} \exp \frac{Q}{K_B T} \tag{1}$$

From the equation (1), it can be observed that the meantime to failure (MTF) of interconnect decreases exponentially with the increase of temperature [15]. The Black equation is used to calculate the MTF for interconnect lines and becomes the typical lifetime assessment method now.

Cu EM and Al EM are significantly different due to their different architectural schemes. While the EM in Al interconnects was well studied. It was found that EM in Al was caused by the diffusion of grain boundary in the 1960s [16]. Under the higher current density, metal ions of interconnect film are prone to spread and diffuse, especially in metal wire with the bamboo structure. It is reported that failure rate caused by EM is extremely high after 0.18um technology node in Al [17]. Nowadays, EM can be predicted by combing the FEA and ANN techniques for ICs [18], [19]. In addition, the introduction of new materials and processing schemes leads to even more challenges in guaranteeing interconnect robustness.

2.1.2. SM failure

Except for EM, the stress-induced-voiding (SIV) or SM is the major failure mechanism which is the result of vacancy movement due to the stress gradient [20]. The stress gradient is the driving force for vacancy diffusion that contributes to the void growth. When interconnect line is placed in the condition of high temperature or no electricity, open circuit is formed by the growth of void and the increase of interconnect resistance [21]. It has been found that large stress builds up and results in the difference of CTE between the metal lines and surrounding dielectrics. The change of temperature in the manufacturing or baking process would form vacancy or cavity nucleation and make the residual thermal stress existed in interconnect system. Areas with the concentrated stress are thought to be the probable spots where voids nucleate. Moreover, the space or hollow is formed along the direction of stress gradient. Generally, SIV occurs at the metal/dielectric interface or via, depending on the properties of the material, geometrical and other aspects related to process.

2.1.3. TM failure

The elevated temperature is the major contributor for reliability degradation. In the micro-interconnect structure, high current which is caused by the geometrical shape of interconnect lines would produce a large number of joule heating and local temperature rise and even temperature gradient. The temperature gradient brings about TM which occurs along the direction of temperature gradient [22]. It is investigated

that the thermo-mechanical stress is the dominant factor and can't be ignored when the line width is below 200 nm. It is reported that TM is found to be the key failure in the 3D interconnect.

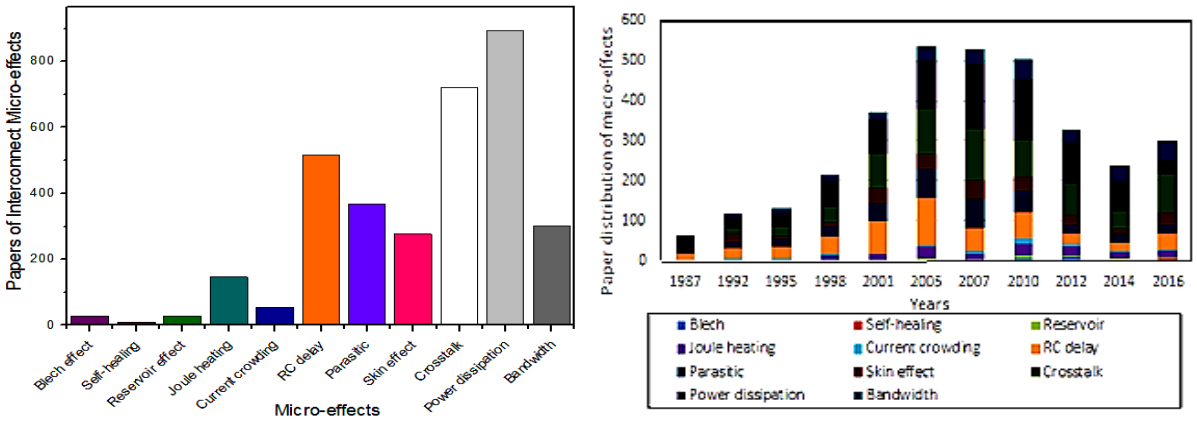
2.1.4. TDDB failure

The TDDB failure in the Cu/ULK interconnect stacks has become one of the most critical reliability issues for state-of-the-art interconnect dielectrics in recent years. TDDB has never been an issue for the Cu/SiO2 interconnects, but when the dimension is below 90 nm, it has become the most serious reliability challenge. TDDB failure is the breakdown related to dielectric materials and time in interconnect system [23]. It is a wear-out of dielectric caused by the electric field and temperature. Under the action of electric field, the drift of Cu ions in dielectric layer directly produces TDDB failure. Extensive efforts are made to solve this issue and several models have been proposed to describe the relationship between electric field and lifetime. Chen did research on TDDB failure and reliability lifetime model for Cu interconnect [24]. Because of the different properties of Cu and Al, the Cu interconnect with barrier layer would bring prominent differences from the Al without barrier layer in TDDB degradation. Due to the decrease of intrinsic breakdown strength of dielectric material, TDDB failure has received extensive concern now.

2.2. Interconnect Micro-effects

The lifetime is the important index to signify the interconnect reliability. With the reduction of feature size and the improvement of working frequency, it is vital to emphasize the interconnect micro-effects which directly influence the interconnect lifetime [25]. For instance, as the operating frequency continues to spiral upward, the interconnect parasitic effect must be considered, which is caused by the increase of interconnect resistivity and capacity. In additional, the problems of delay, power dissipation, bandwidth and noise become more stringent [26].

In addition, a comprehensive analysis of the interconnect micro-effects is given and the paper distribution is illustrated in Fig. 2 (a) and (b). It indicates that parasitic, RC delay, crosstalk and power dissipation have attracted more attention nowadays. Depending on their different effects for failure, these micro-effects are classified into the positive effects and the negative effects.



(a)Nnumber of papers for interconnect micro-effects (b)Paper distribution of interconnect micro-effects

Fig. 2. The statistic of interconnect micro-effects.

2.2.1. Positive effects

A. Short-length effect (blech effect)

In 1976, Blech proposed the famous Blech effect which was also named as the short-length effect. It can be expressed by the equation (2) [27]. Where j is the current density, L is the length of segment, $\Delta\delta$ is the

difference of hydrostatic stress at anode and cathode, Z^* is the effective charge of the Cu, ρ is the resistance of metal, q is the charge of metal, Ω is the atomic volume.

$$(jL)_{Blech} = \Omega \frac{\Delta\delta}{Z^* \rho q} \tag{2}$$

It means that when the product of conductor length (L) and void density (j) is less than a certain threshold, no EM occurs. It has found that shorter Al wires are substantially less susceptible to the EM damage than longer lines when stressed under the same condition [28]. The short-length effect in the DD Cu interconnects has been investigated through the experiments on the lines of different lengths, different current densities in the three-level structure [29].

The product (jL) Blech is determined by the varying metal length and current density [30]. Fig. 3 depicts the decreasing tendency of (jL) Blech with the failure rate, which means that the reliability is improved by (jL) Blech. Moreover, short-length effect has a profound impact on increasing current limit and brings long EM lifetime. In general, jL/B (B is the effective Bulk Modulus) is used as a figure of merit to describe immortality of interconnect lines. However, jL2/B is the correct figure of merit [31]. Therefore, as an accelerated EM factor, (jL) Blech is used to predict EM lifetime. However, *MTF* no longer depends on length when it reaches a certain value.

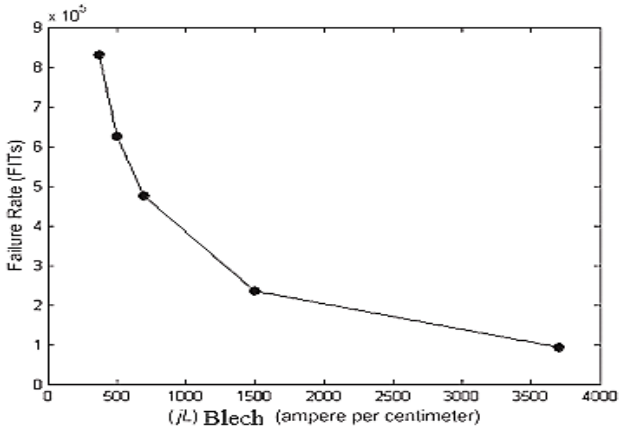


Fig. 3. The trend of (jL)Blech vs. failure rate [30].

B. Self-healing effect (back-flow effect)

EM can cause atomic directed movement then form gradient concentration. Because of the existence of mass gradient, the phenomenon of atoms redistribution is called self-healing or back-flow effect which can reduce EM and repair the EM defects. Because the change of materials is inevitable, so the repair is incomplete. In the case of alternating current or pulse, self-healing effect improves the EM lifetime and is benefit to interconnect reliability [32].

C. Reservoir effect

Reservoir effect means that the part area of metal provides a large number of metal ions which likes an ion library. It is available to fill the missing ions in contact or near vias during EM [33]. In order to compensate the metal ions which are stopped near the borders by the electronic wind migration, it is necessary to control the via formation and expansion. The reservoir area is consisted of the top cap, via area and end lap in MLI structure. It is defined as an extended region of metal line under or over vias.

Reservoir effect has been investigated in the Cu/low-k DD interconnects with the varied length. As interconnect width is continuously shrinking, it is vital to examine if the reservoir effect remains as effective

as the line extension part serves as reservoir of atoms during EM. Nguyen explored the effect of reservoir area on the EM reliability using Al and Cu interconnect respectively [34]. The results reflected the dependency of median time to failure (MTTF) was on the total reservoir area rather than the via pattern. It is reported that the reservoir slows down EM failure and prolongs the interconnect lifetime but up to a certain extend beyond which there is no improvement. Generally, reservoir effect is benefit to improve the interconnect reliability.

2.2.2. Negative effects

A. Skin effect

High density integration makes the conditions of heat dissipation deteriorated constantly. Especially in the signal lines of high frequency, the influence of skin effect is indispensable. The skin effect refers to the exponential reduction of current density along the direction of conductor center and the total current distribution can be equivalent to uniform current distribution in metal layer with a thickness of delta (δ). When the frequency exceeds the certain value, skin effect will occur. A self-consistent method to guide the reliability design of high frequency for a two-level Cu interconnects incorporating the impact of skin effect was presented in [35]. The main intention is to analyze the impact of the signal attenuation induced by skin effect.

B. Joule heating effect (self-heating effect)

As the scaling of IC and the increase of current density, Joule heating has received tremendous attention in interconnect. The impact of Joule heating in metal lines becomes an unavoidable problem. Joule heating which is also named as self-heating is depended on the factors such as current density, interconnect resistivity, ambient temperature, surrounding materials and interconnect design. For example, the metal/Si contacts and inter-layer vias often bear extremely high current density and Joule heating. In the process of signal transmission, the impact of thermal performance cannot be ignored when current flows through the interconnect lines. The heat of the top interconnect is difficult to dissipate and would induce failure. And the Joule heating of the Cu wires can be expressed as equation (3):

$$Q = I_S^2 \rho \tag{3}$$

where Q is the Joule heating, I_S is the current density in Cu lines, ρ is the resistivity of Cu. The rise of temperature and temperature gradient caused by Joule heating has significant influence on the IC reliability. In reference [36] showed the effect of self-heating based on a 4-level interconnect test structure and presented a thermal simulator for the design process. Moreover, it is found that non-uniform current distribution introduces higher power density than the uniform one near contacts. Joule heating also strongly impacts the power dissipation of interconnect which is the another challenge for the complicated IC.

C. Current crowding effect

Fig. 4 shows that current crowding has become remarkable with the improvement of technology. With the increasing current density, the current crowding and current gradient indeed exist in the angled structure. When the current crowding occurs in the Cu and interfaces of barrier layer, EM is intensified. In order to relieve current crowding, the interconnect optimal design is the best choose [37]. Kwok [38] did the pioneer attempt to understand the current distribution in two-level studs and vias. They used the two-dimensional FEM simulation to calculate the distribution of current and temperature in MLI.

In addition, the change of current direction in local area would also cause current crowding and make the path complicated. In the future interconnect system, it is predictable that current crowding will be more significant and its effect on EM should not be ignored.

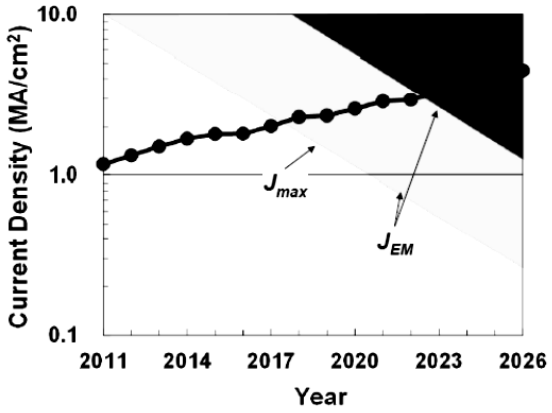


Fig. 4. The general trend of current density.

D. Interconnect parasitic effect

As the increase of interconnect density, interconnect parasitic effect has become the major restrictive factor for realization of high speed, high density, low power consumption, multi-function of IC. The capacitance is the dominant contribution to the parasitic effect and limits the speed of circuit directly. Therefore, in order to reduce the cross-section area of interconnect is the most beneficial measure. In addition, the exploration of new material is inevitable to reduce parasitic effect. For instance, Cu is used to reduce the interconnect resistance and low-k is used to reduce interconnect capacitance. Another method is to analyze the parasitic effect based on some parasitic models. How to build the precise and effective interconnect parasitic model has become the focus for interconnect design. In addition, the inductive effect began to be highlighted in the distributed RLC equivalent circuit model with the nano-scale CMOS process.

E. RC delay

In parallel, the interconnect delay is becoming the limitation of the overall signal propagation. The total resistance (R) of the interconnect structure is now a significant factor affecting the chip performance. At the same time, the capacitance (C) between wires is increasing due to the decreasing spacing between wires. Both factors significantly increase the RC delay of IC. Nowadays, the limitation to IC reliability is not the gate delay of device, but the interconnect delay which is caused by the parasitic components. The interconnect resistance and capacitance between metal layers are the major parasitic components, which directly decide the RC delay. That is to say by reducing total resistance and capacitance can decrease the interconnect delay. The RC delay in interconnect wires can be calculated by the equation (4) as follow:

$$RC_{delay} = 2\rho k\varepsilon_0 L^2\left(\frac{1}{W^2}+\frac{1}{T^2}\right) \tag{4}$$

where L is the length of interconnect line, T is the height of metal, W is the thickness of metal, ρ is the resistance of metal, k is the dielectric constant, ε_0 is the dielectric constant of vacuum. When the working frequency increases to GHz, the parasitic inductance greatly aggravates the interconnect delay. When feature size decreases to 0.18 um, the restriction on chip speed has shifted from the gate delay to interconnect delay. Then RC delay has exceeded the gate delay of intrinsic transistor, which is the main bottleneck restricting IC performance. As the feature size continues to shrink below 0.13 um, the RC delay has become the major restriction for interconnect performance. When feature size further narrows to 50 nm, RC delay has brought a series of problems such as parasitic effect, crosstalk and power consumption. The variation trends of interconnect delay and gate delay are depicted in Fig. 5.

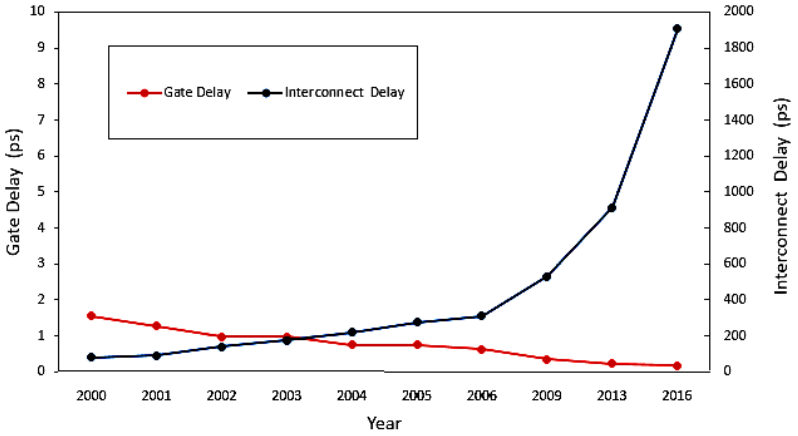


Fig. 5. Gate delay and interconnect delay versus year.

RC delay severely impacts the interconnect performance. Therefore, it is necessary to take measures to optimize delay. It is reported that the efficient methods to reduce RC delay include using low-k dielectric, inserting repeater and increasing line width [39]. The first approach to reduce interconnect delay is to improve the interconnect materials. The silicate and Cu can help to reduce resistance of polycrystalline silicon and metal wire. Low-k dielectric is used to reduce capacitance. It is widespread to use the Cu and low-k in advanced CMOS process. As the Fig. 6 shown, different interconnect structures have different RC delay and gate delay, especially the Cu/air-gap structure has the lowest RC delay. However, the new materials generally can keep only one or two generations, delay has not been solved thoroughly. To update technology is the only way to deal with the delay.

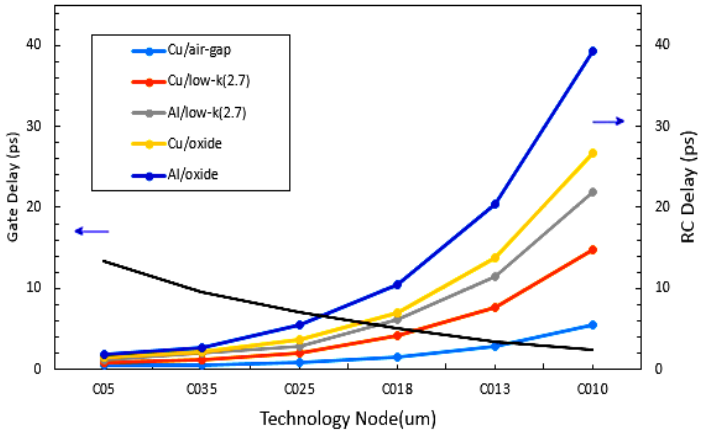


Fig. 6. Gate delay vs. RC delay in different interconnect structures.

With the development of CMOS technology, the global interconnect delay which was once significantly small has become hundreds of times of the transistor delay in the complicated system. The conventional method to reduce the long wire delay is to insert the repeater. As the Fig. 7 shown, the gate delay for local and global with or without repeater is quite different. However, it also brings some problems such as the intrinsic delay, power dissipation and expenditure of silicon area. By changing wire width to reduce interconnect delay is the another optimization method. However, the increase of line width results in large interconnect capacitance and brings some difficulties for layout. Therefore, how to optimize the interconnect delay is still a challenge for interconnect reliability.

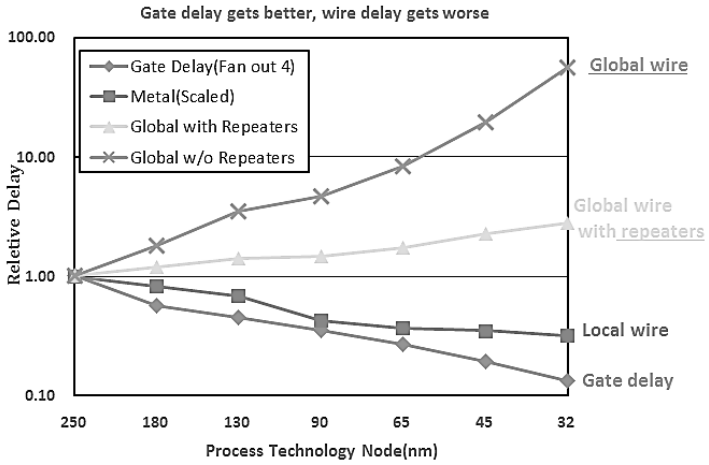


Fig. 7.The delay for local and global gate delay with/without repeater.

F. Crosstalk and coupled noise

When the peak value of interference noise induced by the electromagnetic coupling between the adjacent lines is big enough, logic chaos of transmission signal occurs and makes the terminal load out of order [40]. The crosstalk and coupled noise are the potential failure in high speed electronic system. What is more, crosstalk would change effective characteristic impedance and system delay. Meanwhile, the signal integrity is also destroyed by the crosstalk and noise.

G. Interconnect power dissipation

With the tendency of miniaturization and function integration, the interconnect density and power dissipation increase obviously. Circuit designers must minimize the parasitic capacitance to reduce the power dissipation and improve circuit speed. In 2012, ITRS pointed out that the layer number of interconnect has reached 13, interconnect length of IC has accumulated up to 103 m, while the power dissipation of individual IC continues to increase [41]. It indicates that power dissipation has become new focus for interconnect reliability. In addition, interconnect power dissipation increases greatly and occupies a large proportion of the whole power dissipation. It directly impacts the integration and reliability of the system.

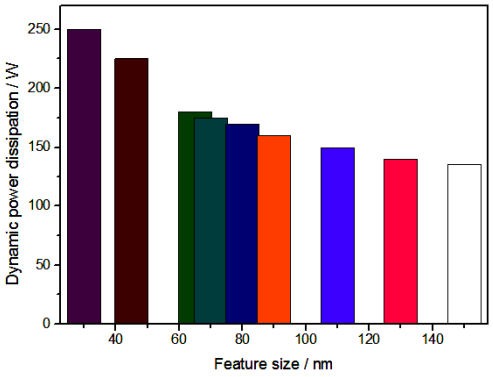


Fig. 8. The trend of dynamic power dissipation.

Interconnect power dissipation includes the dynamic, static and short circuit power dissipation. The dynamic power dissipation is caused by the switch flipping which occupies a large part. It is reported that dynamic power dissipation increases dramatically with the scaling of feature size as the Fig. 8 shown. To forecast and reduce the power dissipation have become the critical subject for today's IC design. It is reported that using model to compute and optimize power dissipation is prevailing [42].

H. Interconnect bandwidth

The bandwidth is the amount of data which is transmitted in chip per unit time. For a given chip, the interconnect bandwidth is the function of unit delay and the number of interconnect and it is given by the equation (5):

$$\phi = \frac{1}{(W+S)\frac{T_{total}}{L}} \tag{5}$$

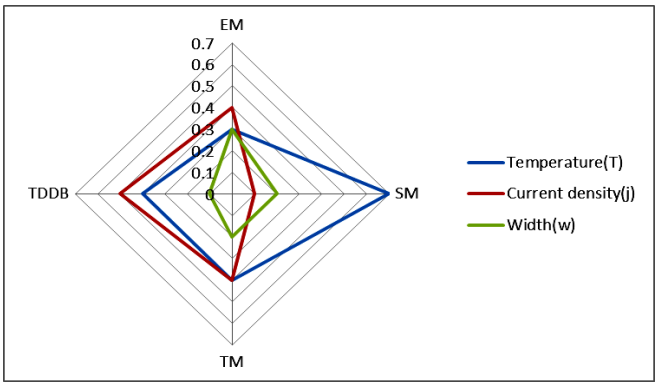
where ϕ is the interconnect bandwidth, W is the line-width, S is the line thickness, L is the line length, T total is the total delay time. Due to the increase of signal frequency, the improvement of bandwidth has become the important part for high speed IC. The target of interconnect design is to obtain larger bandwidth and keep acceptable delay of unit length as far as possible. The large bandwidth means big data throughput and the small delay means high performance interconnect. To increase line width and line spacing is effective to reduce delay at the expense of part bandwidth. They can't reach the optimal value at the same time and need to make the reasonable compromise.

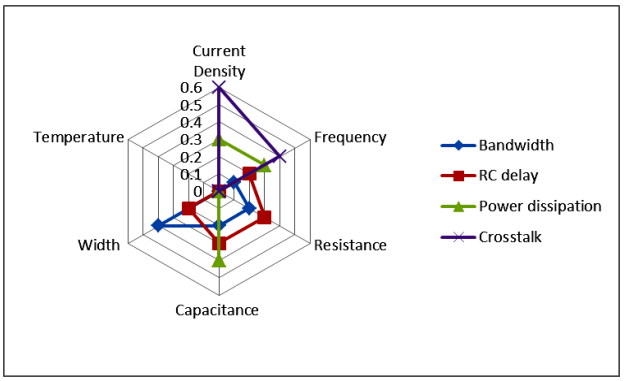
2.3. Evaluation Method

How to evaluate these failure mechanisms and micro-effects in interconnect reliability? Various factors ought to be taken into account, such as the current density, frequency, resistance, capacitance, width and temperature and so on.

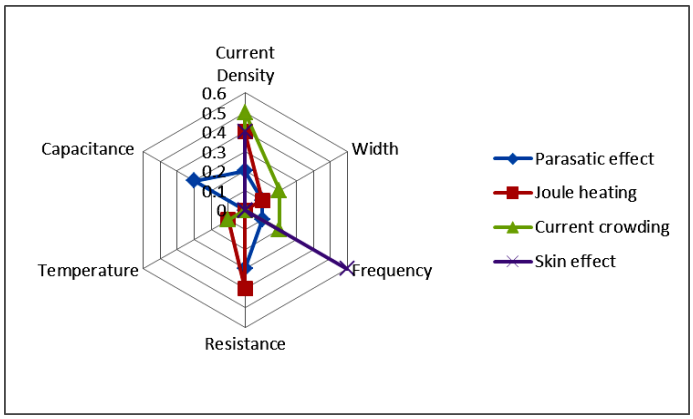
In general, the interconnect micro-effects is divided into two sets, which are related to performance failure and physics failure. The RC delay, crosstalk, power dissipation and bandwidth belong to the physics failure, while Joule heating, current crowding, parasitic effect and skin effect belong to the performance failure. It is reported that current density, temperature, frequency, width, resistance and capacity are the key factors to decide these micro-effects. In order to evaluate the extent, a novel qualitative evaluation method has been put forward-radar chart. Every radial axis represents a performance index and the distance represents the extent of impact.

Take the failure mechanisms for example, by scoring for the factors according the extent of impact. The radar chart is as the Fig. 9 and 10 shown respectively, the longer the wire, the greater the impact. From the Fig. 9 (a) we can see that temperature is the major impact and width is the minimum impact for failure mechanisms. From the Fig. 10 (a), it is found that EM accounts for the maximum proportion for interconnect reliability.



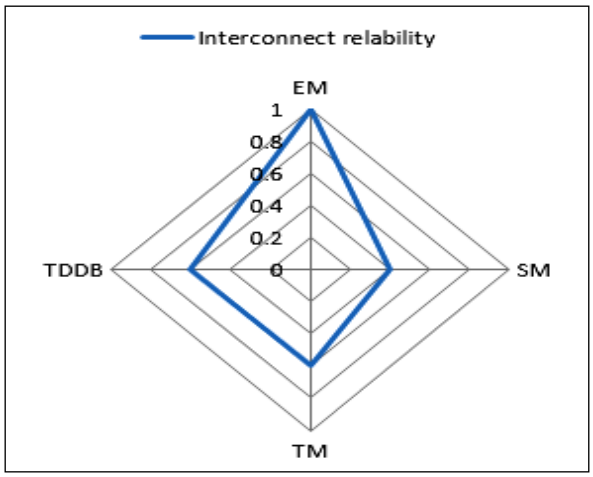


(a) The factor distribution of failure mechanisms (b) The factor distribution of performance failures

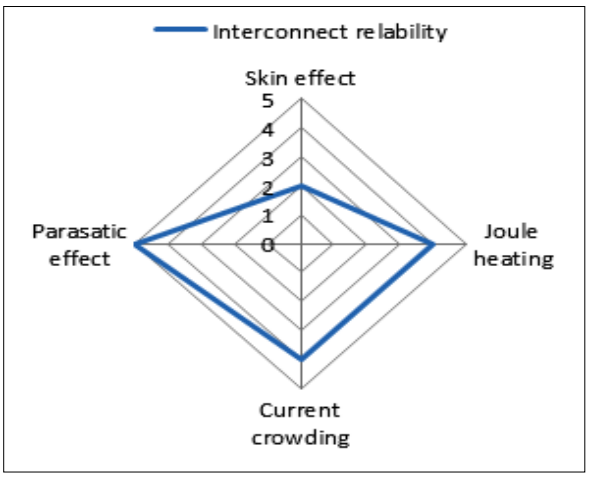


(c) The factor distribution of physics failures

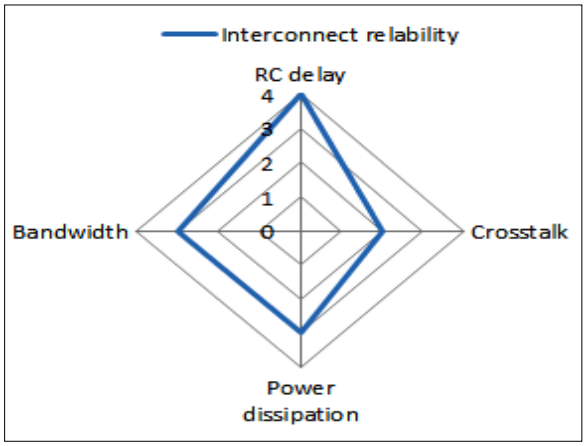
Fig. 9. Key influences on failure mechanisms and micro-effects.



(a) Failure mechanisms for interconnect reliability



(b) Physics failure for interconnect reliability



(c) Performance failure for interconnect reliabiliy

Fig. 10. The influence distribution of failure mechanisms and micro-effects for interconnect reliability.

In the case of micro-effects, the radar chart is as Fig. 9 (b) and (c) shown, the longer the wire, the greater the impact. From the Fig. 9 (b) and (c) we can see that impact distribution for the performance failure and physics failure. From the Fig. 10 (b) and (c) it is shown that parasitic effect and RC delay account for the maximum proportion for interconnect reliability.

In order to study the failure behavior, the usage of model is necessary. Meanwhile, with the variation of

interconnect structure the process changes are of crucial importance. Therefore, the interconnect modeling and the process changes need to be taken into account in the interconnect challenges. According to the figures above, we can clearly identify the impact of failure mechanisms or micro-effects for the interconnect reliability. When certain factor varies, it is easy to trace the related failure mechanisms or micro-effects. In turn, when failure occurs, we can quickly pay attention to the certain factors. It is effective to find the reasons for any failures. All these can give some guidance to control failures.

3. Conclusion

An overview of IC interconnect reliability has been presented. In general, the failure mechanisms and micro-effects for interconnect are analyzed and summarized here. Moreover, a novel qualitative evaluation method has been presented, which visually show the contrast of these failure mechanisms and micro-effects.

With the development of semiconductor industry, the technical and physical extremity would be broken by exploring new materials and new technologies. Moreover, the interconnect parasite, crosstalk noise and RC delay have become the most difficult challenges for IC. All these can provide some valuable guidance for the study of IC interconnect reliability.

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