

SOCD Sort on Centralized Diamond Architecture

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Abstract: Parallel sorting is a technique which researchers have studied from the time parallelism was proposed as a way of making fast algorithms. Different parallel sorting techniques on different architectures have been studied for many years. Sorting is one of the most important operations in different algorithms. This paper presents another sort on Centralized Diamond architecture which sorts unsorted lists of length L . The theoretical analysis of the algorithm specifies that the algorithm needs $o(\log n)$ time complexity on PRAM EREW.

Key words: Sorting, centralized diamond, SIMD, EREW PRAM.

1. Introduction

Parallelizing can save time and solve very large problems in computational tasks. Parallelism provides concurrency which is used to solve problems such as time consuming sort. Some sorting algorithms are given in [1], [2]. Parallel architectures are made up of multiple processors and memory modules that are connected together using some interconnection networks [3]. Interconnection network is an important core of digital parallel processing systems [4]. The definitions of Diamond are first presented in [5]. There are various parallel algorithms on Diamond architecture with different specifications in [6]-[9].

Centralized Diamond is an SIMD architecture which has four subsection including EREW, ERCW, CREW, and CRCW [10]. There are lots of processors that provide a set of Single Instruction Multiple Data (SIMD) instructions including the VMX instruction set or the SSE instruction set. Such processors can do multiple operations on multiple blocks of data in parallel to speedup CPU intensive parts of applications which includes a wide variety of applications. Availability of data parallelism degree in one instruction is an obvious advantage of the SIMD [11]. Centralized Diamond has $7/4n+1$ processor elements. The sorting algorithm presented in this paper is on unsorted lists of input data with length of L .

In this algorithm, the k-merge algorithm which sorts k sorted list with $O(\log n)$ on EREW PRAM [12] is employed. The PRAM is used widely for parallel computation. It was developed to do parallel computing operations like the RAM does for sequential computing and ignores the communication issues [13].

The rest of the article is organized as following. In the next section, interconnection networks are summarized. After that, the proposed algorithm is presented. Then, the time complexity and the cost of the proposed algorithm are discussed. Finally the conclusion is drawn.

2. Interconnection Networks

Interconnection networks are divided into static and dynamic. Dynamic interconnection networks are also called indirect [14]. In dynamic interconnections, the connections are set up on the fly according to the

needs. Based on the interconnection scheme, dynamic interconnections are divided into switch-based and bus-based.

There are different kinds of static interconnection networks including completely connected network (CCN) which is expensive due to many interconnections and limited connected network (LCN). The latter is divided into one-dimensional (1D), two-dimensional (2D), three-dimensional (3D), four-dimensional (4D), and hybrid. As opposed to the dynamic INs, the static interconnection networks have fixed connections.

In CCNs, all PEs have one direct path to all other PEs. Therefore, they are expensive because of the links which are in need. The links' count in a CCN with N PEs is $N(N-1)/2$, which is $O(N^2)$ [3]. In these interconnection networks, the diameter is one and the degree of this topology is $O(N)$ [3], [15].

In LCNs, linear array is the simplest one-dimensional limited interconnection network. Each PE is connected to its two neighbors. The common 2D interconnection networks include mesh, tree, ring, fat tree, ILLIAC, and torus. The 3D interconnection networks are designed in the form of cube. Cube is one of the most practical interconnection networks among existing interconnection networks. The most well-known 4D interconnection networks is Hypercube topology because of its properties such as strong connectivity, topological symmetry, regularity, and recursive constructions. Hybrid topologies such as mesh of trees and pyramid are combination of the other basic topologies including meshes and trees. Centralized Diamond is a hybrid interconnection network which has appropriate connections between processor elements (PEs). It is composed of tree and ring interconnection network. An example of different types of limited interconnection networks is drawn in Fig. 1.

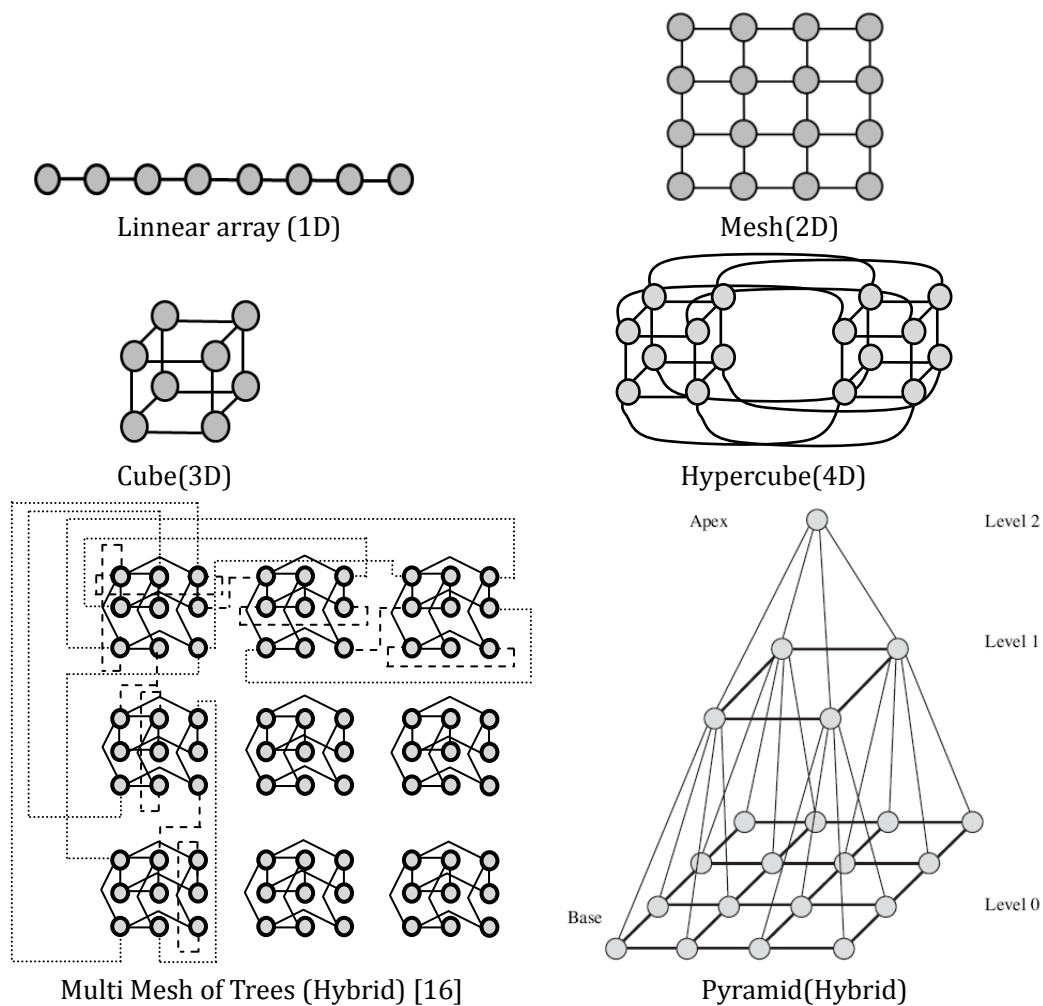


Fig. 1. Examples of static interconnection network topologies.

One of the most important factors with high impact on IN performance is topology [17]. While there are different architectures with different specifications, researchers choose the topology which is more appropriate for their algorithm considering the specifications of the architecture.

3. Sorting on Centralized Diamond Architecture

Assume that N is the number of processor elements, and L is the length of each unsorted list which is given to the third level of Centralized Diamond. Only one layer of the processor elements of the architecture are dealing with the data at each step. The steps of doing the sort are described in the following.

Step 1: Each PE gets its unsorted list with length of L as it is shown in Fig. 2. This figure is drawn for $N=29$ and $n=16$. The length of unsorted lists is considered to be three. The number of processor elements is $7/4n+1$. This architecture has four levels where level three has n PEs, level two has $n/2$ PEs, and level one has $n/4$ PEs. Finally, level zero there has only one processor element which is called centralized PE. In the third level, each PE has direct connectivity to the processor elements next to it. The relation is as following:

$$x \geq 3n/4 \quad \text{where } x \bmod 2 \neq 0$$

$$\Pi_{+1}(x) = x + 1$$

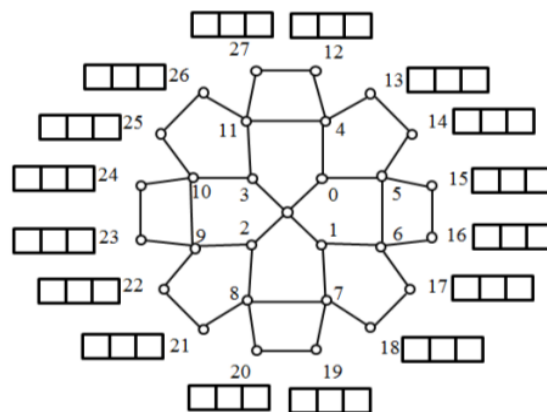


Fig. 2. Entrance of unsorted lists with length $L=3$ to the third level.

Each PE has adequate registers to store data elements. In addition, each PE has registers for sorting data elements in it. Therefore, each PE in the third level has $2L$ registers. Each PE in the third level sorts its data elements using parallel merge sort with $O(\log L)$ time complexity where $L \ll n$. This operation is illustrated in Fig. 3 considering $L = 7$.

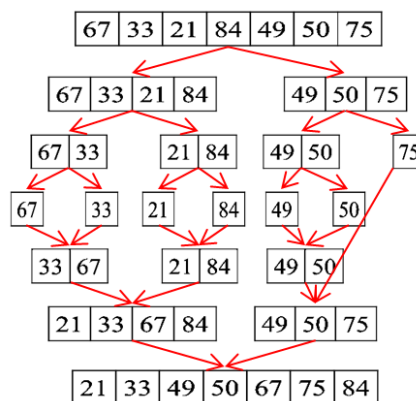


Fig. 3. Parallel merge sort in the PEs of the third level.

Step 2: At the beginning of this step, each PE in the third level has a sorted list. Using k-merge sorted list from [12] with $O(\log n)$ time complexity, the data elements of third level are sorted in the second level of the architecture. In the second level, each processor element is connected directly to the processor element next to it. The relation is as following:

$$\begin{aligned} n/4 \leq x \leq 3n/4 \\ \Pi_{+1}(x) &= x + 1 \\ \Pi_{+n/4}(x) &= 2x + n/4 \quad \text{where } x \bmod 2 \neq 0 \\ \Pi_{+n/4+1}(x) &= 2x + n/4 + 1 \end{aligned}$$

Fig. 4 shows a small part of the whole architecture to perform this operation including PEs 18, 19, and 7.

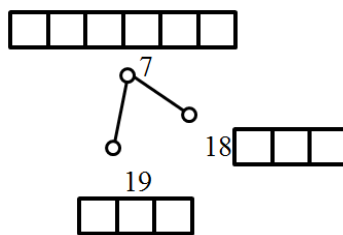


Fig. 4. Merging sorted list of level three using k-merge sort.

Step 3: Each PE in the second level has a sorted list with length of $2L$. The data elements of second level are merged with the k-merge sorted list algorithm and the sorted data are located in the first level. In the first level, each PE is connected directly to the centralized node. The equations are as following:

$$\begin{aligned} x &< n/4 \\ \Pi_{+n/4}(x) &= 2x + n/4 \\ \Pi_{+n/4+1}(x) &= 2x + n/4 + 1 \end{aligned}$$

To simplify the understanding, a part of the architecture is presented in Fig. 5 including PEs, 16, 17, 18, 19, 6, 7, and 1 which performs the operation of this step.

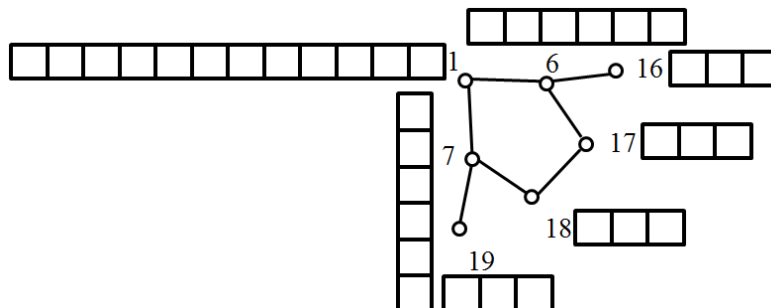


Fig. 5. Merging sorted list of level two using k-merge sort.

Step 4: The centralized PE merge sorted data elements of the first layer using k-merge sort which needs $O(\log n)$. This level has only one processor element. Length of each list is $4L$. The final list in the centralized PE is the sorted list. The length of the list for this example is $16L$.

The flowchart of the proposed algorithm is presented in Fig. 6. Following the steps for unsorted input lists, the sorted list will be achieved.

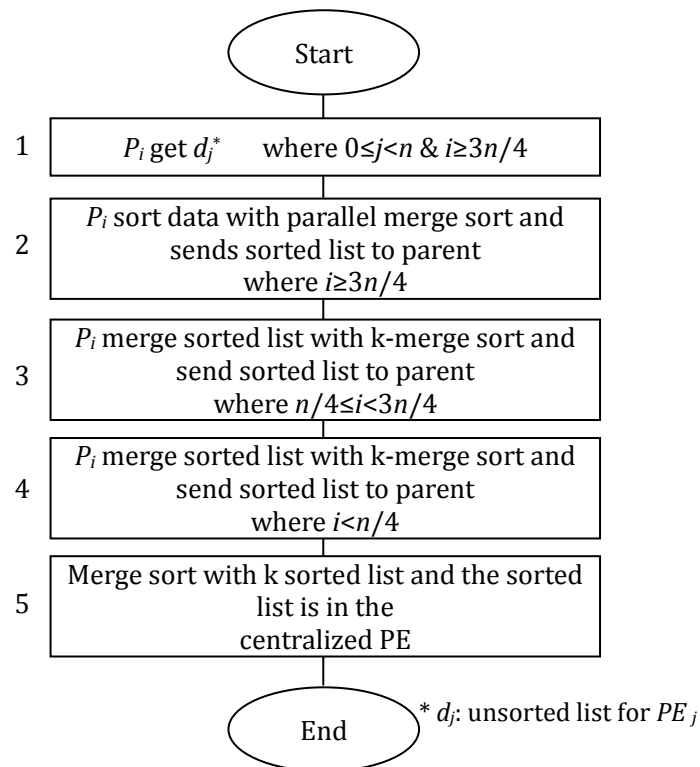


Fig. 6. Flowchart of the sorting algorithm.

4. Time Complexity and Cost

In the proposed sorting algorithm and from the flowchart in Fig. 6, step one has a time complexity of $O(\log L)$ and each of steps 2, 3, 4 and 5 has a time complexity of $O(\log n)$. The overall time complexity is $O(\log L) + O(\log n) + O(\log n) + O(\log n)$ where $L \ll n$. Therefore, the total execution time is $O(\log n)$. The number of processor elements that are used for execution of the algorithm is called p_n . If the processor elements are equal to the number of data elements, all the data can be fed into the system simultaneously. In this algorithm number of data elements are more than PEs, which can be calculated using

$p_n = O\left(\frac{7}{4}n + 1\right) = O(n) = O(N)$. The time from the start of the first processor element to the end of the last

processor element for executing the algorithm is the parallel time. This is the number of basic operations for the longest path. The parallel time in this algorithm is $t_n = O(\log n)$. The total time which the processor elements use to execute the algorithm is the total cost. If the parallel time is $t(n)$ and the number of processors is $p(n)$, then the total cost will be $C(n) = t(n) \times p(n)$. The total cost is $c_n = O(n \log n)$.

5. Conclusion

We proposed a sorting algorithm on unsorted input lists using Centralized Diamond architecture. The type of interconnections of this architecture affects the results of sorting in terms of speed and time complexity. The Centralized Diamond architecture is composed of ring and tree which has suitable specifications such as logarithmic diameter. The proposed sorting algorithm needs $O(\log n)$ time complexity. This algorithm has an appropriate order. The architecture is heterogeneous, which means the

capabilities of PEs in the leaves are different from the PEs in other levels. This fact does not affect the synchronization of processing because the processor elements are the same at each level, therefore they finish their operation at the same time.

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