Architecture and Design of High Speed Data Acquisition System

Cao Bin, Chong Ming Ying, Kyaw Swa Maung, Lai Yoon Fei, Manoj Kumar Dey, and Sandeep Dattaprasad

***Abstract*—Data acquisition systems are of interest for purposes such as parametric measurement and verification of data integrity, particularly for high speed memory devices such as DDR. This paper analyzes and proposes a simple principle and structure for designing one such hardware system with use of Field Programmable Gate Arrays (FPGAs). A hardware system employing this architecture is illustrated here using E2V's Analog to Digital Converters (ADC), Altera's Stratix III and Cyclone II FPGAs and Samsung's 1Gb DDR3 memory devices for data storage.**

***Index Terms*—Data acquisition, high speed, field programmable gate array, ADC, DDR.**

I. Introduction

With development of faster memory devices such as DDR3 being able to achieve data rates of 1600 Mb/sec (DDR3 – 1600), measurement of critical parameters on the fly such as - Clock rise and fall time, setup / hold time, timing information related to Data strobe (DQS), has become imperative to judge the quality of the memory device and to analyse the root cause of memory failures.

Though such measurements may be taken with high speed oscilloscopes and logic analysers, as the number of memory devices on a board increases, the accuracy of measurement and the feasibility of measurement may be compromised. In addition, high speed oscilloscopes and logic analysers are not cost effective solutions. Therefore, there is a strong need for a data acquisition system which can be used as an add-on card which caters to the above described measurement challenges.

For applications such as DDR whose data and timing parameters to be measured are in several GHz range, maintaining signal integrity on the board involves various challenges such as matching the lengths of the traces, impedance requirements, matching terminations and avoiding reflections. With increase in devices such as FIFOs and Demux on the board, it would be much more complex to meet these requirements on a PCB with no advantage in performance.

In the past development of such acquisition systems have largely been based on de- multiplexers (Demux) and FIFOs for de serialising and capturing, as illustrated in figure 1, for an 8 bit ADC.

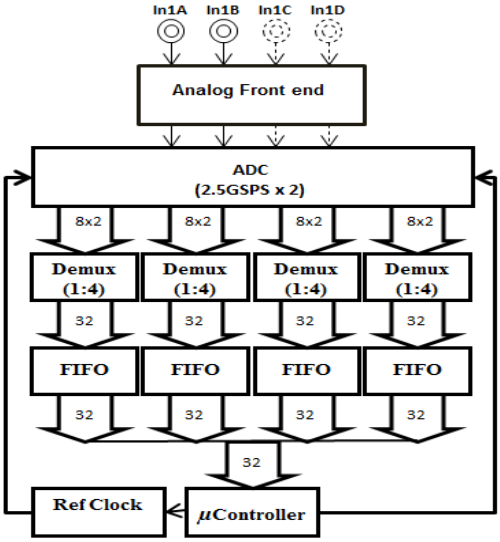

Fig. 1. FIFO based acquisition system

However, as evident from Fig. 1, use of de-mux and FIFOs for large number of channels not only increases the cost and but also space on the Printed Circuit Board (PCB). In consideration of all the above factors, a new architecture of acquisition system using advanced, high-performance, low-power FPGAs which are specifically designed for ease of use and rapid system integration for high speed applications is presented in this paper. The main purpose of this high speed signal acquisition system is for measuring critical timing parameters of high speed devices.

II. Architecture

Figure below illustrates an acquisition system using Altera's Stratix III and Cyclone II FPGAs.

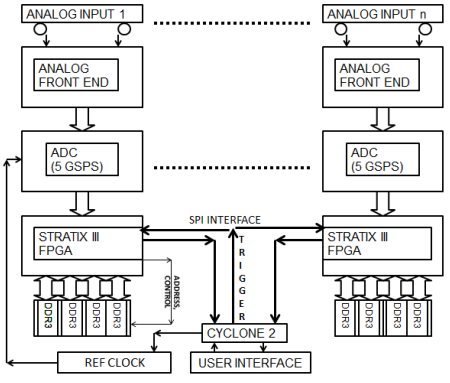

Fig. 2. Acquisition system architecture

Stratix III acts as a primary FPGA which is responsible

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for acquiring data from specific ADC while Cyclone II is responsible for generating control signals necessary. This is explained in detail in the following sections.

A. Analog Front End (AFE) / Trigger Circuit

The analog input to the acquisition system can be from any high speed memory or interface device operating at data rates above 1 GHz. The purpose of the circuit is to feed the incoming high speed data in to ADC through a multi- stage Operational Amplifier and at the same time generate trigger signal at which the input signals are to be sampled. The trigger signal is generated upon meeting specific timing condition which is based on samples from multiple input channels. The trigger reference voltage is set by a second FPGA (Cyclone II). Trigger thus generated is used to capture the pre trigger and post trigger events from ADC samples. The basic circuitry is shown in the block diagram below:

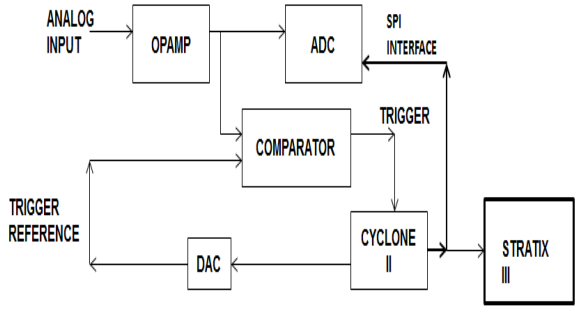

Fig. 3. AFE / Trigger circuit blocks

B. Analog to Digital Converter (ADC)

The ADC used in in our experiments was E2V's EV8AQ160 Quad ADC. This ADC is constituted by four 8-bit ADC cores. It can be set up in single, dual or four channel mode. In One-channel mode the maximum sampling rate of 5GSps can be achieved.

Depending in the number of ADCs used and number of channels used in each ADC, fan out buffers for the clock circuit must be used since a common clock needs to drive all the ADCs. In our experiments since 4 ADCs were used, all four ADCs are clocked by the same external input clock signal. The ADC is controlled via SPI interface through Cyclone II, to set it up in required modes and to provide the 2.5Ghz (max) reference clock.

C. Field Programmable Gate Arrays (FPGA)

As described earlier, the FPGAs are the core of architecture. Instead of sending the incoming ADC data to external FIFOs and Demux, it is sent to embedded FIFOs and De-Serialisers inside the FPGAs.

Altera's Stratix III was used for this purpose. The FIFOs and De-Serialiser IPs are generated using Megacore® function in Quartus II. Stratix III supports high-speed external memory interfaces including DDR, DDR2, and DDR3 SDRAM. It also supports high-speed differential inputs and outputs running at speeds up to 800 MHz and 500 MHz, respectively. The large number of clocking resources, in combination with the clock synthesis precision provided by the PLLs, provides a complete clock management solution in Stratix III. The Quartus II software enables the PLLs and their features without requiring any external devices. Considering all these features and resources, we found Stratix III to be an ideal FGPA for this application.

The data acquired from different ADCs will be processed in Stratix III and stored in an external DDR3 memory device. The main function of this FPGA is to buffer the incoming ADC data, facilitate reading/writing from/to the memory through the user interface. The data thus collected can then be retrieved and sent to a second FPGA or microcontroller which takes care of processing requests by the user interface.

For ease of use and flexibility, Cyclone II was used as the second FPGA in this application. Cyclone II has high-speed differential I/O standard support, including LVDS which makes it easy to use with Stratix III. In addition, it is compliant with 3.3-V *PCI Local Bus Specification, Revision 3.0* for 3.3-V operation at 33 or 66 MHz for 32- or 64-bit interfaces and has PCIe interface with an external TI PHY and Altera PCI Express ×1 Megacore® function. This makes it ideal for interfacing with an external computer.

D. Memory Interface

To store the high speed data processed from Stratix III FPGA, we need a high speed memory from which we can read and write to easily. Stratix III supports DDR3 memory interface and has memory controller IPs that can be used and adjusted easily. The Quartus II software has ALTMEMPHY Megafunction, which is an interface between a memory controller and the memory devices, and performs read and write operations to the memory as shown in figure below.

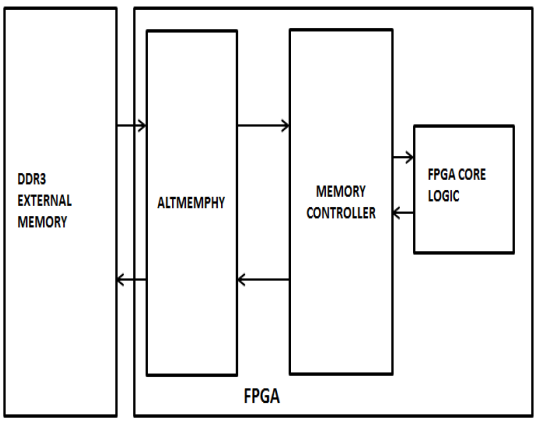

Fig. 4. Altera DDR3 memory controller

The DDR3 SDRAM Controllers works in conjunction with the Altera ALTMEMPHY IP. The ALTMEMPHY Megafunction creates the data path between the memory device and the memory controller. ALTMEMPHY IP is a part of the Megacore® IP Library, which is distributed with the Quartus II software. So, no additional cost is incurred for interfacing with DDR3 memories. The MegaWizard Plug-In Manager flows allows customizing the DDR3 SDRAM High-Performance Controller Megafunction, and manually integrate the function into the design. DDR3 controller writes to and reads from four 16-bit DDR3 RAMs. Samsung K4B1G1646 DDR3 memory device was used for this application. The 1Gb DDR3 SDRAM C-die is

organized as a 64Mbit x 16 with 8 banks per device. This synchronous device achieves high speed double-data-rate transfer rates of up to 1333Mb/sec/pin (DDR3- 1333) for general applications.

The chip is designed to comply with the key DDR3 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset.

E. Software interface

The software interface can be broadly divided into two parts:

1) Device Driver - Provides a communication link between the high-level application software and the low-level hardware components. It is responsible for setting the PCI configuration space to communicate with the PCI interface of Cyclone II FPGA. In addition it issues read requests and maintains the various register settings for ADC, PLL and other programmable devices on board.

2) GUI Application - Handles the user inputs, processes the data captured from the ADCs, and provides the visual feedback to the end-user. The user can also configure the ADCs separately so as to measure different types of signal through the use of a sequence file (text-based).

The software interface described here is PCI- based. However, depending on the communication interface between FPGA and the host PC, this can be written for USB, PCIe or any other PC interface protocol.

III. Design Challenges

Design of an acquisition system has various hardware design challenges.

There can be noise/interference generated from the internal electronic components. Sources include ADC conversion process noise and harmonic distortion, buffer amplifier noise and distortions, and reference noise and in-stability. Important factors for choosing an amplifier for 8-bit to 16-bit accuracy are: sufficient bandwidth, slew rate, V_{P-P} output, low noise, low distortion, and low offset. Buffer amplifier noise must be kept as low as possible—far below the SNR of the ADC. Anti-aliasing and noise-suppression low pass filters is needed on each input channel of the ADCs. Filter components should also be located as close as possible to ADC inputs. Power pins need to have sufficient bypass capacitors compensating for different noise frequency components. Each ADC has 64 LVDS pairs, need to be of equal lengths. LVDS pairs need impedance controlled.

DDR3 Memory interface: 80 data lines, 24 command / clock / address. In case of DDR3, a data/address signal is always transmitted along with its corresponding strobe/clock signal to minimize skew.

This is especially critical in designs that target the top-end interface speeds, because the data switches at twice the applied clock frequency. To ensure signal integrity on data lines, each data lane needs to be adjacent to a solid ground reference for the entire route to provide the lowest inductance for the return currents.

The fly-by termination architecture of the DDR3 DIMM reduces the number of simultaneous switching signals but causes flight-time skew, which can be up to two cycles across the DIMM. Therefore, a write "leveling" feature was defined in DDR3 memories to enable controllers to compensate for this skew by adjusting the timing per byte lane. The write leveling needs to enabled and set up while generating the memory controller and ALTMEMPHY through Altera's Megafunction.

In addition, to compensate for any skew in the signals, Stratix III has I/O programmable delay elements which are constructed and staggered for coarse and fine tuning of delays. This helps to skew or de-skew data signals to or from a bus of pins to compensate for process variations in the die, package, circuit board and external interfacing devices. This is advantageous especially at sampling frequencies higher than 4 GSps (single channel mode), since due to the internal signal path skew inside the FPGA, occasionally some of the signals are skewed compared to the rest causing bit flip issues.

To compensate for this, the respective data signals can be de-skewed by using the programmable delay elements inside the FPGA. Variable input and output delay can be used to compensating for trace length mismatch and electrical de-skew. The delay elements can be reached from the FPGA fabric at run time to implement automatic DDR3 de-skew algorithms as part of the start-up calibration process. To choose appropriate delays for the design, the amount of skew on different signal lines can be known through "Delay Chain Summary report" after compilation in Quartus software.

IV. Advantages of this Architecture

1) High accuracy of measurement of signals up to 4 GSps.
2) Cost effective compared to use of high speed oscilloscopes and logic analyzers.
3) Using FPGAs instead of FIFOs saves space and improves the signal integrity on board.
4) Design has the flexibility to accommodate as many acquisition channels as needed at a modest increase in PCB area.
5) Since the entire architecture is modeled as an add-on card, it is extremely easy to use and accommodates on the fly measurement of critical signals.

V. Conclusion

The architecture described above was successfully implemented and tested for accuracy of measurement up to 4 GSps. The data from a high speed ADC was acquired and the timing parameters of a DDR device were measured successfully.

At sampling rates above 4 GSps, the internal delay and skew on the signal path through the FPGA plays a major factor in maintaining the precision of measurement. Some additional work to assess this design challenge is being pursued.

REFERENCES

[1] Z. Peyton Peebles, Jr. "*Digital Communication Systems*," Prentice-Hall, INC.

[2] J. Shtargot, "*Design Guidelines for High-Performance,* Multichannel*, Simultaneous-Sampling ADCs in Data-Acquisition Systems*," Maxim semiconductors.

[3] P. Murray, A. Corporation, and F. A. Hawari, Cadence Design Systems, Inc. "*Challenges in implementing DDR3 memory interface on PCBsystems: a methodology for interfacing DDR3 SDRAM DIMM to an FPGA*," DesignCon 2008.

[4] Datasheet, "*Samsung 1Gb E-die DDR3 SDRAM specification*," Samsung electronics, Rev. 1.0 Febraury 2009

[5] Application note, "*Implementing Stratix III, Programmable I/O Delay Settings in the Quartus II Software*," Altera Corporation, March 2008, Ver.1.2.

[6] Application note, "*Stratix III Design Guidelines*", Altera corporation, May 2008 Version 1.1.

[7] Datasheet, "*Stratix III Device Datasheet: DC and Switching Characteristics*," Altera Corporation.

[8] Datasheet, "*Cyclone II Device Family Data Sheet*," Altera Corporation.

[9] Datasheet, "*EV8AQ160 Quad ADC*", e2v technologies plc.

[10] Double Date Rate (DDR) SDRAM Specification, JEDEC Standard No.79C